WHAT IS CLAIMED IS

1. A semiconductor integrated device comprising a ROM decoder of n bits for selecting one gradation voltage out of gradation voltages of the n-th power of 2 gradation in connection with data signals of n bits (n represents an integer of 2 or more) representing a gradation level, said ROM decoder having n pairs of confronting gate wires each into which the data signal is input with the non-inverted state on one of the pair and with the inverted state on another of the pair,

wherein pairs of the n-th power of 2 each of which comprises an enhancement type transistor and a depletion type transistor kept under ON-state are arranged at predetermined positions one side by one side at the pair of the confronting gate wires, and with respect to each of the pair of the confronting gate wires, the width of the gate wire that contains the upper portion of the depletion type transistor and extends from the depletion type transistor to the enhancement type transistor adjacent to the depletion type transistor is reduced so that recess portions are formed inside the confronting gate wires.

2. A semiconductor integrated device comprising a ROM decoder of n bits for selecting one gradation voltage out of gradation voltages of the n-th power of 2 gradation in connection with data signals of n bits (n represents an integer of 2 or more) representing a gradation level, said ROM decoder having n pairs of confronting gate wires each into which the data signal is input with the non-inverted state on one of the pair and with the inverted state on another of the pair,

wherein pairs of the n-th power of 2 each of which comprises an

enhancement type transistor and a depletion type transistor kept under ON-state are arranged at predetermined positions one side by one side at the pair of the confronting gate wires, and with respect to each of the pair of the confronting gate wires, the width of the gate wire that contains the upper portion of the depletion type transistor and extends from the depletion type transistor to the position between the depletion type transistor and the enhancement type transistor adjacent to the depletion type transistor is reduced so that recess portions are formed inside the confronting gate wires.

3. The semiconductor integrated circuit device according to claim 1, wherein with respect to each of the pair of the confronting gate wires, the width of the gate wire between continuously-arranged depletion type transistors is reduced so that recess portions are formed inside the confronting gate wires.

4. The semiconductor integrated circuit device according to claim 2, wherein with respect to each of the pair of the confronting gate wires, the width of the gate wire between continuously-arranged depletion type transistors is reduced so that recess portions are formed inside the confronting gate wires.

5. The semiconductor integrated circuit device according to claim 1, wherein the reduced width of the gate wire is equal to a half of the gate wire width on the enhancement type transistor.

6. The semiconductor integrated circuit device according to claim 2, wherein the reduced width of the gate wire is equal to a half of the gate wire width on the enhancement type transistor.

7. A liquid display device comprising the semiconductor integrated circuit

device according to claim 1.

8. A liquid display device comprising the semiconductor integrated circuit device according to claim 2.